D3

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 841 751 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
13.05.1998 Bulletin 1998/20

(51) Int Cl.[6]: H03K 5/13

(21) Application number: 97308371.0

(22) Date of filing: 21.10.1997

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

(30) Priority: 06.11.1996 US 744810

(71) Applicants:
- International Business Machines Corporation
  Armonk, N.Y. 10504 (US)
- KABUSHIKI KAISHA TOSHIBA
  Kawasaki-shi, Kanagawa-ken 210 (JP)

(72) Inventors:
- Hara, Takahiko
  Yokohama, Kanagawa 235-0022 (JP)
- Quader, Khandker Nazrul
  Sunnyvale, CA 94087 (US)
- Watanabe, Yohji
  Yokohama, Kanagawa 253 (JP)

(74) Representative: Ling, Christopher John
IBM United Kingdom Limited,
Intellectual Property Department,
Hursley Park
Winchester, Hampshire SO21 2JN (GB)

(54) Delay circuit

(57) According to the preferred embodiment of the invention, an Address Transition Detector (ATD) pulse generating mechanism is provided that overcomes the limitations of the prior art by compensating for process and power supply voltage variations that would normally effect the pulse width. In particular, the delays used to create the pulse width are adjusted to compensate for the effects of process and environmental variations, thereby providing a pulse width that is relatively constant over these variations.

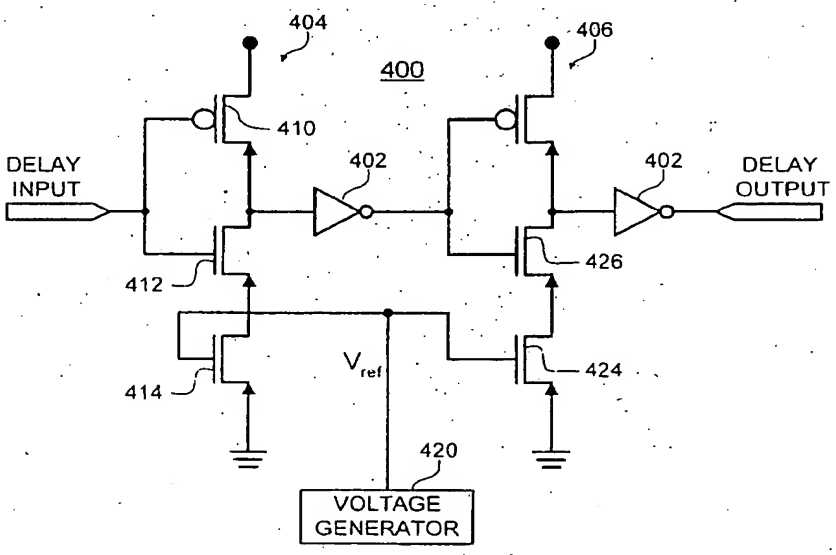

FIG. 4

EP 0 841 751 A1

Printed by Jouve, 75001 PARIS (FR)

Description

TECHNICAL FIELD

This invention generally relates to semiconductor devices, and more specifically relates to timing circuits in semiconductor memory systems.

BACKGROUND ART

Many modern semiconductor devices use timing signals that require accurate pulse widths. Unfortunately, as the operating speed of modern devices increases, the required pulse width often narrows and the task of maintaining an accurate pulse width becomes more difficult. This is especially true where temperature, voltage and process variations potentially affect the signal pulse width.

Most modern memory systems use an address transition detector (ATD) to control the memory circuits such that their evaluation efficiency is maximized. On detecting an address transition, the ATD provides an ATD signal that comprises a pulse or set of pulses. This ATD signal is used to equalize, preset and/or recover the timing critical circuits of the semiconductor memory system, resulting in faster access times. The pulse width of these ATD signals is critical. If the pulse width is too short, it can lead to incorrect data. If the pulse width is too long, the access time may be pushed out (*i.e.*, increased).

Turning now to FIG. 1, FIG. 1 is a portion of a prior art ATD pulse generator 100. ATD pulse generator 100 comprises a plurality of delay elements, including delay elements 102 and 104, a plurality of logic circuits, including logic circuit 106, and an ATD sum 108. The ATD pulse generator receives a plurality of address signals ADDR(i) (e.g., ADDR(1)) and plurality of address signal complements ADDRbar(i) (e.g., ADDRbar(1)) and uses these address signals to create an ATD pulse signal. Typically, the ATD pulse generator 100 receives each address signal in the memory system. For simplicity, FIG. 1 illustrates only the ADDR(1) inputs, with the ADDR(2) to ADDR(i) inputs not shown. The address signals and address signal complements are each split and sent through an ADDR(1) delay element 102 and an ADDRbar(1) delay element 104 resulting in ADDR(1)DLY and ADDRbar(1)DLY signals. The resulting four signals are inputted to a logic circuit 106. The logic circuit 106 performs an exclusive OR operation on each set of two signals and then performs an OR operation on the results. This results in an ATD(1) signal that is outputted to ATD sum 108.

Similar elements create ATD(2) through ATD(*i*) and these signals are all inputted to ATD sum 108. ATD sum 108 is preferably a full CMOS or ratioed NOR device. Thus, ATD sum 108 "ORs" the ATD(*i*) signals, creating the final ATD signal.

Turning now to FIG. 3, FIG. 3 is a waveform diagram of various signals in ATD pulse generator 100. The waveforms include two address signals (ADDR(1) and ADDR(2)) and their complements. Also shown are two delayed address signals (ADDR(1)DLY and ADDR(2)DLY) and their complements. Of course, in an actual ATD device, many more address signals (ADDR(3)-ADDR(i)) would be used to create the ATD signal.

ADDR(1), ADDR(1)DLY and their complements are inputted into a logic circuit 106 which outputs an ATD(1) signal. Likewise, ADDR(2), ADDR(2)DLY and their complements are inputted into a logic circuit (not shown in FIG. 1) which outputs an ATD(2) signal. As shown in FIG. 3, the ATD(*i*) signals have a pulse width that is a function of the delay through the various delay elements (e.g., 102, 104). These ATD(*i*) signals, are summed together by ATD sum 108.

Thus, the ATD pulse width is determined by the amount of delay through the delay elements. The accuracy of the pulse width is then a function of the accuracy of the delay elements.

Turning now to FIG. 2, FIG. 2 is a schematic view of delay element 200. The delay element 200 is a typical prior art delay that is used in ADDR delay 102 and ADDRbar delay 104 of FIG. 1. Delay element 200 comprises strings of inverters 202 with capacitors 204 in between. The delay through the inverters 202 determines the width of the ATD pulse. Unfortunately, the use of inverters 202 to determine the ATD pulse width has the disadvantage of creating pulse widths that can vary with process and environmental changes. Specifically, because the delay through inverters is a function of process variations, temperature and power supply voltage, the final pulse width of the ATD signal will also fluctuate with those parameters. Without the ability to control the effects of this variation, the ATD pulse width cannot be accurately provided, especially where a short ATD pulse width is required. Thus, this variation can limit the performance of the memory system.

To try and compensate for this problem, some prior art approaches for optimizing ATD pulse width includes trimming the ATD pulse width during fabrication to compensate for process variations. This solution however, does not compensate for variations in the power supply voltage and operating temperature of the memory system. Other solutions have used longer pulse widths to compensate for variations. Unfortunately, this approach comes at the expense of access time and is not an optimal solution.

Therefore, there existed a need to provide an improved mechanism for providing an accurate ATD signal having an optimized pulse width that avoids the limitations and problems of the prior art.

DISCLOSURE OF INVENTION

According to the present invention, an ATD pulse generating mechanism is provided that overcomes the limitations of the prior art by compensating for process

and power supply voltage variations that would normally affect the pulse width. In particular, the delays used to create the pulse width are adjusted to compensate for the effects of process and environmental variations, thereby providing a pulse width that is relatively constant over these variations.

BRIEF DESCRIPTION OF DRAWINGS

The invention will now be described by way of example only, with reference to the accompanying drawings, in which like designations denote like elements, and:

FIG. 1 is schematic view of a portion of a prior art ATD pulse generator 100;

FIG. 2 is a schematic view of a prior art delay element 200;

FIG. 3 is a waveform diagram of various signals in prior art ATD pulse generator 100;

FIG. 4 is a schematic view of a delay element 400 in accordance with the preferred embodiment of the present invention; and

FIG. 5 is a schematic view of a reference voltage generator 420 in accordance with the preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The preferred embodiment of the present invention provides a pulse generator that overcomes the limitations of the prior art. In particular, the pulse generator comprises a delay element that provides consistent delay by compensating for process and power supply voltage variations that would normally change the delay. For example, in the prior art, as the temperature of the pulse generator decreased, the delay through the delay elements would also decrease, and could result in too narrow a pulse width. In a pulse generator in accordance with the preferred embodiment, a temperature dependent current source controlled by a reference voltage V_{REF} is used to mitigate the effects of such a temperature decrease by increasing the delay through the delay elements.

Turning now to FIG. 4, FIG. 4 is a schematic view of a delay element 400 in accordance with the preferred embodiment of the present invention. The delay element 400 can be used as delay elements 102 and 104 of FIG. 1, providing a more accurate pulse generation.

The delay element 400 comprises two conventional inverters 402 and two compensated inverters 404 and 406. Together, the four inverters provide a delay from input to output of delay element 400.

Compensated invertor 404 comprises a P-FET 410, an N-FET 412 and an N-FET 414. A reference voltage V_{REF} is supplied to the gate of N-FET 414 from voltage generator 420. The compensated inverter 404 operates as follows: the reference voltage V_{REF} controls the maximum amount of current that can flow through N-FET 414. Thus, as V_{REF} increases or decreases, the current that can flow through N-FET 412 and N-FET 414 increases or decreases respectively.

The delay through inverter 404 is dependent upon the maximum current that can flow through N-FETs 412 and 414 during signal transition. Thus, when V_{REF} increases N-FET 412 and N-FET 414 increase their current, causing the delay through inverter 404 to shorten. Likewise, when V_{REF} decreases, the current through N-FETs 412 and 414 decreases, causing the delay through invertor 404 to increase. Thus, the N-FET 414 acts as a temperature dependent current source controlled by a reference voltage V_{REF} Voltage generator 420 varies V_{RFF} with temperature to compensate for temperature-induced changes in the delay of inverter 404, thereby maintaining a relatively constant delay through inverter 404 over a wide temperature range.

V_{REF} controls the delay through invertor 406 in a like manner. In particular, adjusting V_{REF} adjusts the current through N-FET 424 and N-FET 426. Thus, by adjusting the reference voltage V_{REF} the delay through the delay element 400 can be adjusted to compensate for temperature and other variations. This allows for the ATD pulse width to be kept constant over a wide range of temperature and power supply voltage variations.

In the preferred embodiment, two inverters in the prior art delay circuit are replaced with compensated invertors. In particular, those inverters that provide delay where the input makes a transition from low to high are replaced. Those skilled in the art will recognize that the other inverters could be similarly replaced if desired or necessary.

Turning now to FIG. 5, FIG. 5 is a schematic view of a voltage generator 420. The voltage generator 420 is designed to provide reference voltage V_{REF} for the compensated inverters 404 and 406 of FIG. 4. In one embodiment, the voltage generator 420 is a modified band gap reference circuit. Band gap reference circuits are commonly used to provide an accurate band gap reference voltage V_{BGR} for a wide variety of applications. The voltage generator 420 has been modified to provide a reference voltage V_{REF} for the compensated inverters 404 and 406 in addition to the V_{BGR}. Thus, in applications where a band gap reference voltage V_{BGR} is required, a voltage generator 420 can provide V_{BGR} in addition to V_{REF} with only a relatively small amount of additional circuitry.

The voltage generator 420 comprises a first diode coupled transistor 502, a second diode coupled transistor 504; resistors 506, 508 and 510; a differential amplifier 512; a plurality of P-FETs 514, 516 and 518; and an N-FET 520.

The diode coupled transistors 502 and 504 are se-

lected to provide an accurate voltage drop based on the semiconductor band gap. Diode coupled transistor 504 has preferably ten times the semiconductor area as diode coupled transistor 502, and hence ten times the emitter current density. Differential amplifier 512 controls the current flowing through P-FETs 514 and 516 such that the voltage levels V_1 and V_2 at its input become equal. This causes a reference current, I_{REF} to flow through diode coupled transistor 504. If P-FETs 514 and 516 are identical, two resistors 508 and 510 should also be identical, resulting in the current through the diode transistors 502 and 504 being the same.

Based upon the current equation for diode coupled transistors, the reference current I_{REF} is as follows:

$$I_{REF} = \frac{kT \ln (X)}{qR}$$

where k is Boltzmann's constant, T is temperature in degrees Kelvin, q is an electron's charge, R is the resistance of resistor 506 and X is the ratio of emitter current density in transistors 504 and 502 (preferably 10). Thus, if the resistor 506 is selected to have resistance R with no temperature dependence, the current I_{REF} flowing through diode coupled transistor 504 is proportional to ambient temperature. The current I_{REF} is mirrored through P-FETs 516 and 518, causing a current I to flow through N-FET 520. If P-FETs 516 and 518 are identical. current I will be equal to I_{REF}. If P-FETs 516 and 518 are different, current I and $_{IREF}$ will have different values, but the ratio of currents I/I_{REF} will be kept constant. Since the current I_{REF} is proportional to temperature, current I is also proportional to temperature.

Where V_{BGR} is to be used as a reference voltage by other circuits, resistors 508 and 510 are preferably selected to have ten times the resistance of resistor 506 to effectively eliminate a temperature dependence of the V_{BGR}.

Returning to FIG. 4, with V_{REF} connected to the gates of N-FETs 414 and 424, the current I of FIG. 5 will be mirrored from N-FET 520 into the inverters 404 and 406. The current flowing through inverters 404 and 406 will then be proportional to the temperature in the same way that the current I is. In particular, as the temperature goes down the mirrored current through inverters 404 and 406 will decrease as well. Thus, the voltage generator 420 is designed to provide a reference voltage V_{REF} adapted to reduced the drive to N-FETs 414 and 424 (of FIG. 4) at lower temperatures. This reduces the change in the delay element's delay that would normally occur at lower temperatures, hence reducing the amount of pulse width variation that would normally occur at such a temperature.

Furthermore, since the current I does not depend on the transistor characteristics, the mirrored currents flowing through the N-FETs 414 and 424 do not vary even if the process parameters (i.e., threshold voltage Vt) vary as long as the mirror FETS (414, 424, and 520) all experience the same process. In order to improve this mirror effect, it is preferable to choose the same gate length for all FETS which make up the current mirror so that a gate length variation gives those FETS the same current variation in ratio.

In general the maximum ATD pulse width occurs in slow conditions, such as high temperature, low power supply voltage, and long response due to process variations. In the prior art, the pulse width narrows as conditions speed up, such as lower temperature, higher power supply voltage and shorter response due to process variations. Because the preferred embodiment compensates for the effects of faster conditions, the ATD pulse generator can be designed to have a minimum but adequate pulse width at slow conditions without having too narrow a pulse width under fast conditions. This improves the speed at which the device can be designed to operate. In particular, V_{REF} is used to assure that the ATD pulse width does not overly narrow and is adequate under fast conditions.

It should be understood that, while various of the conductors are shown in the drawing as single lines, they are not so shown in a limiting sense, and may comprise plural conductor, as is understood in the art.

Claims

1. A circuit for generating a pulse having a pulse width, the circuit comprising:

   a) at least one delay element (400), said delay element comprising at least one compensated inverter (404, 406), said compensated inverter having a propagation delay that at least partially defines said pulse width and wherein said propagation delay can be adjusted by means of a reference voltage (Vref) ; and

   b) a reference voltage generator (420) for generating said reference voltage, wherein said generator adjusts said reference voltage to compensate the propagation delay of said compensated inverter for temperature variations.

2. A circuit as claimed in claim 1 wherein said reference voltage generator (420) comprises a first diode (504), said first diode in series with a substantially temperature independent impedance (506), said impedance and said first diode having a reference current proportional to temperature, said reference current being mirrored to create said reference voltage.

3. A circuit as claimed in claim 2 further comprising a second diode (502), said second diode having one tenth the semiconductor area of said first diode (504).

4. A circuit as claimed in claim 3 further comprising an amplifier (512), said amplifier driving said first (504) and second (502) diodes such that the current I_{REF} flowing though said first diode is:

$$I_{REF} = \frac{kT \ln (X)}{qR}$$

where k is Boltzmann's constant, T is temperature in degrees Kelvin of said circuit, q is an electron's charge, R is the resistance of said impedance, and X is ratio of emitter current density in said first diode to said second diode.

5. A circuit as claimed in claim 1 wherein said delay element (400) comprises two inverters (402) and two compensated inverters (404, 406).

6. A circuit as claimed in claim 1 wherein said reference voltage (Vref) adjusts to reduce the drive of said delay elements (404, 406) when said temperature variations comprises a temperature decrease, and wherein said reference voltage (Vref) adjusts to increase the drive of said delay elements (404, 406) when said temperature variations comprise a temperature increase.

7. A circuit as claimed in claim 1 wherein said circuit comprises an address transition detector and wherein said pulse comprises an address transition detector pulse.

8. An address transition detector pulse generator for generating address transition detector pulses each having a pulse width, the address transition detector pulse generator comprising:

a circuit as claimed in any preceding claim, said circuit partially defining said pulse width of said address transition detector pulses, said compensated inverters in said circuit having a propagation delay that partially defines said pulse width and wherein said propagation delay can be adjusted by means of a reference voltage.

9. A method for compensating for the effects of temperature variations on propagation delay in a pulse generating circuit, the method comprising the steps of:

a) providing a plurality of delay elements (400), each of said plurality of delay elements comprising at least one compensated inverter (404, 406), said compensated inverter having a propagation delay that partially defines the pulse width and wherein said propagation delay can be adjusted by means of a reference voltage (Vref) ; and

b) adjusting said reference voltage to compensate the propagation delay of said inverter for temperature variations.

10. A method as claimed in claim 9 wherein the step of adjusting said reference voltage (Vref) comprises providing a reference current I_{REF} flowing through a diode (504) and an impedance (506), wherein said reference current I_{REF} comprises:

$$I_{REF} = \frac{kT \ln (X)}{qR}$$

where k is Boltzmann's constant, T is temperature in degrees Kelvin of said pulse generating circuit, q is an electron's charge, R is the resistance of said impedance and X is a constant.

11. A method as claimed in claim 9 wherein the step of adjusting said reference voltage (Vref) to compensate said inverter (400) for temperature variations comprises reducing the drive of said delay elements when said temperature variations comprises a temperature decrease, and wherein the step of adjusting said reference voltage to compensate said inverter for temperature variations comprises increases the drive of said delay elements when said temperature variations comprises a temperature increase.

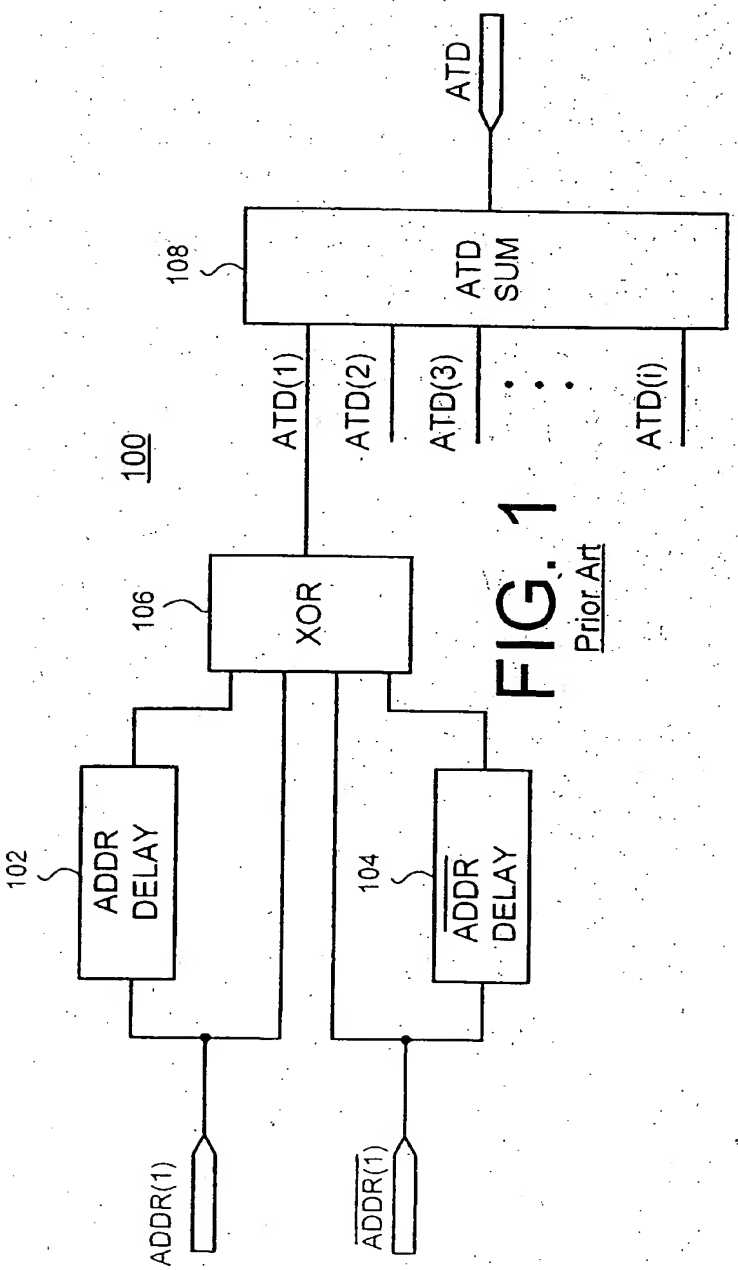

FIG. 1
Prior Art

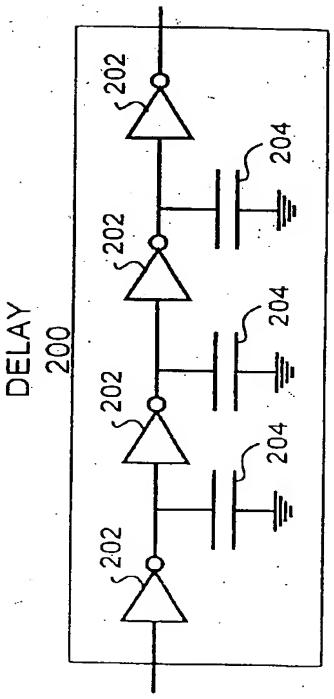

FIG. 2
Prior Art

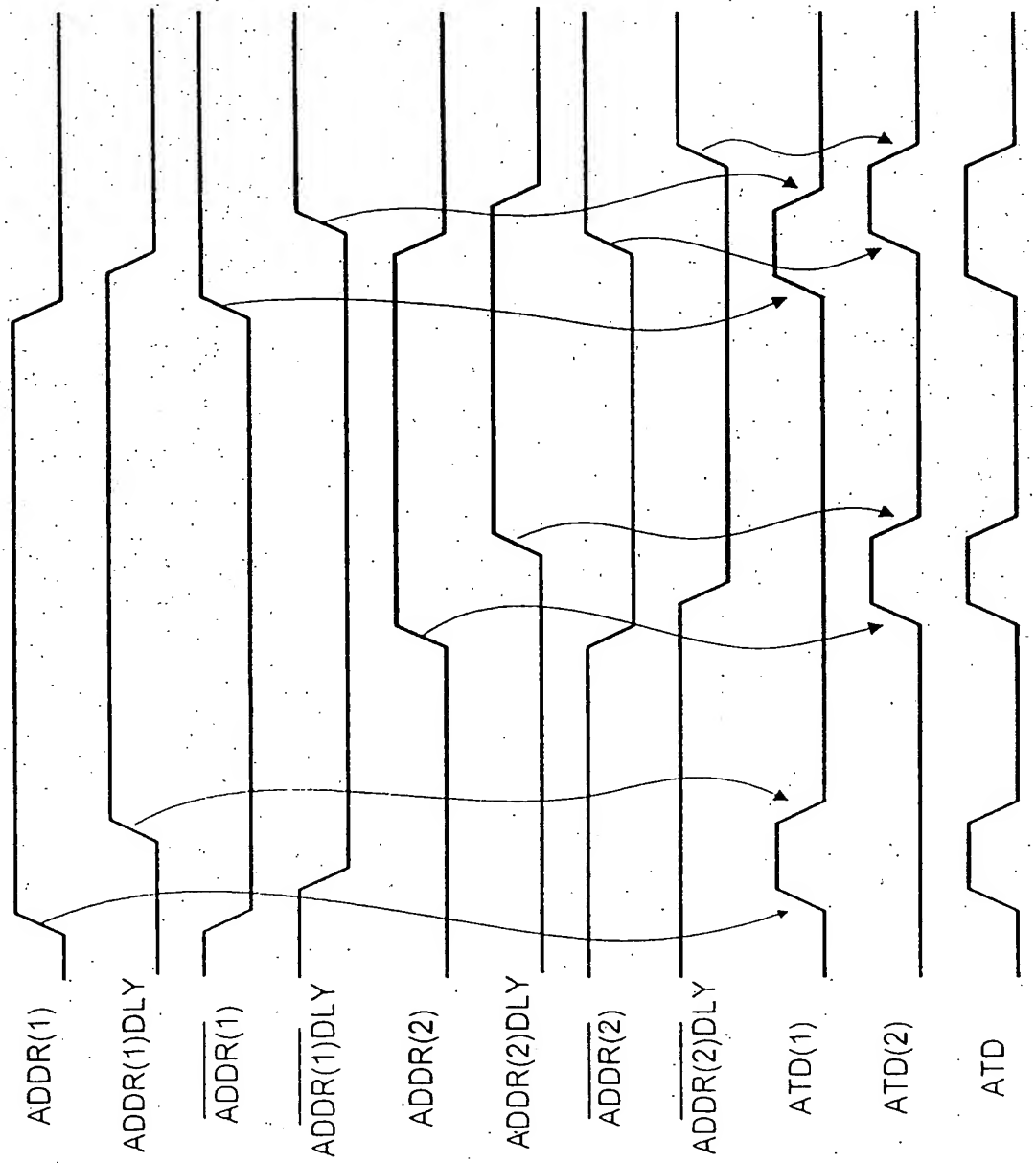
ADDR(1)
ADDR(1)DLY
$\overline{\text{ADDR(1)}}$
$\overline{\text{ADDR(1)DLY}}$
ADDR(2)
ADDR(2)DLY
$\overline{\text{ADDR(2)}}$
$\overline{\text{ADDR(2)DLY}}$
ATD(1)
ATD(2)
ATD

FIG. 3

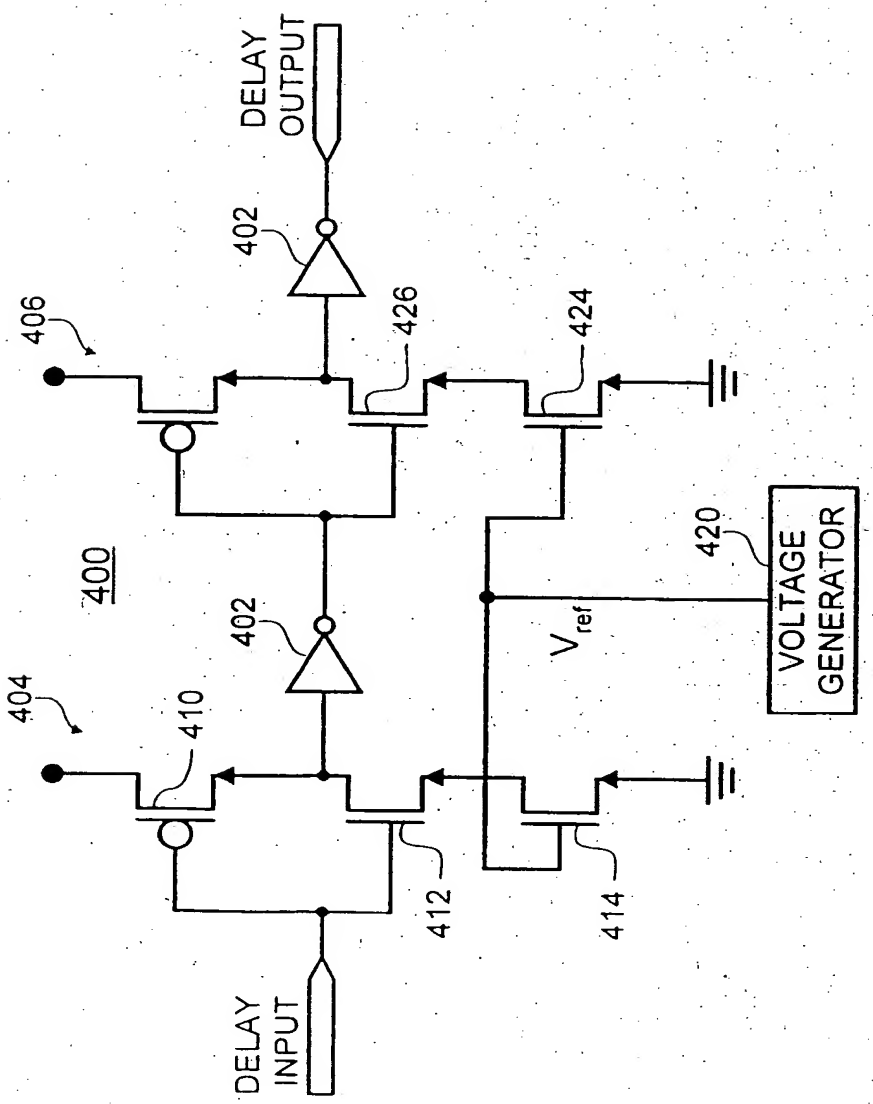
DELAY OUTPUT
402
406
426
424
400
402
420
VOLTAGE GENERATOR
V_{ref}
404
410
412
414
DELAY INPUT

FIG. 4

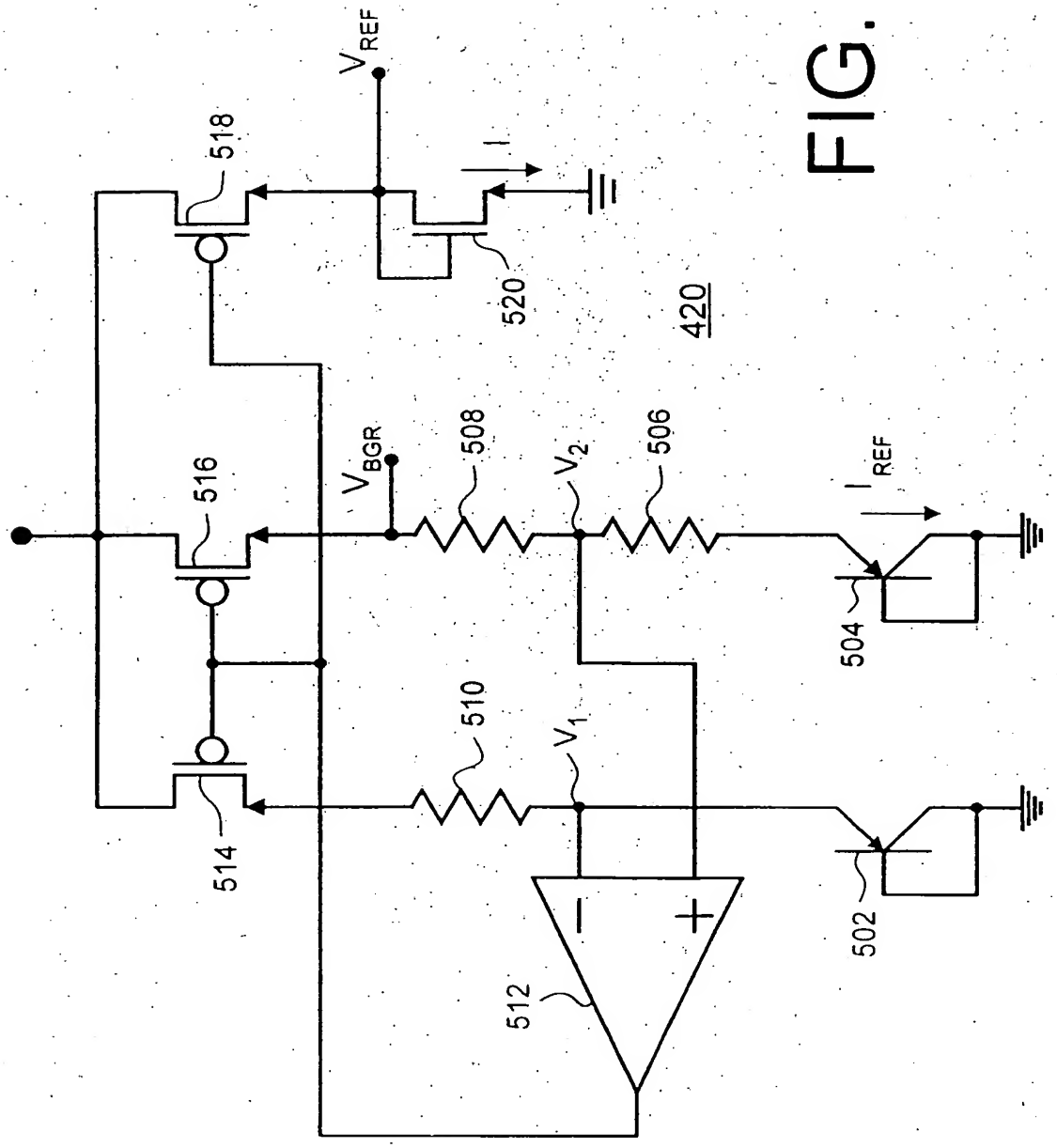
V_{REF}
518
I
520
420
V_{BGR}
508
V_2
506
I_{REF}
516
504
510
V_1
514
502
512

FIG. 5

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 30 8371

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X Y	US 5 164 621 A (MIYAMOTO TAKAYUKI) * the whole document * ---	1 2-11	H03K5/13
Y	EP 0 698 841 A (SGS THOMSON MICROELECTRONICS (GB)) * abstract; figure 2 * ---	2-11	
A	US 5 180 930 A (MAYES MICHAEL K) * abstract; figure 3 * ---	1-11	
A	US 5 231 320 A (KASE KIYOSHI) * abstract; figures 2,4 * ---	1-11	
A	EP 0 423 963 A (ADVANCED MICRO DEVICES INC) ---		
A	EP 0 566 375 A (NOKIA MOBILE PHONES LTD) -----		

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H03K
G11C
G05F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	16 February 1998	Segaert, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)